Amendments to the Specification

Please amend the paragraph at page 7, line 23 through page 8, line 13 as follows:

The control signal generating circuit 20 generates a control signal C having a "high" level when the number of data bits which are simultaneously input or output is more than a predetermined bit number (e.g., [[3]]18-bits) and generates a control signal C having a "low" level when the number of data bits is less than a predetermined bit number (e.g., 18-bits). When a control signal C having a "low" level is generated, the PMOS transistor P1 is turned on, and the NMOS transistor N1 is turned off. The comparator 10 and the PMOS transistor P perform the same operation as described in FIG. 1. That is, an internal voltage IVC level becomes a reference voltage VREF level. On the other hand, when a control signal C having a "high" level is generated, the PMOS transistor P1 is turned off, and the NMOS transistor N1 is turned on. An external power voltage EVC is cut off, so that operation of the comparator 10 is disabled, and a node A becomes a "low" level. As a result, the PMOS transistor P is turned on, so that an internal voltage IVC becomes an external power voltage EVC level.